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Crystal Growth and Wafer Preparation

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Crystal Growth and Wafer Preparation

2.0 Introduction

In this chapter, we shall discuss two aspects of microelectronics manufacturing, which covers the methods used to grow silicon crystal and how the growth crystalline silicon is prepared into silicon wafer for fabrication into integrated circuits.

2.1 Crystal Growth

Before the fabrication of the integrated circuit, the preparation of silicon or gallium arsenide wafer is required. The preparation of wafer involves several process steps. They are distillation and reduction/synthesis, crystal growth, grind/saw/polish, and electrical and mechanical characterizations. We shall not discuss the process of making gallium arsenide GaAs wafer. We shall concentrate on the process of making silicon wafer.

The starting material is silicon dioxide for making silicon wafer. It is chemically processed to form a high-purity crystal polycrystalline semiconductor for which single crystal is formed. The single crystal ingot is shaped to define diameter and is sawed into wafer. The wafer is then etched and polished to provide smooth, specular surface where device is fabricated.

Pure form of sand SiO_2 called *quartzile* is placed in high temperature furnace with various forms of carbon like coke, coal, and even wood chip. Owing silicon dioxide is very stable, carbon is used to replace silicon to form carbon dioxide at reduce temperature. Although there are numbers of reaction take place and the overall reaction follows equation (2.1).

$$SiO_2 + 2C \rightarrow Si + 2CO\uparrow \qquad (2.1)$$

This process generates polycrystalline silicon with about 98% to 99% purity called *crude silicon* or *metallurgical-grade silicon* MGS.

In next process step is the silicon purification step. Silicon is pulverized and treated with hydrochloric acid gas HCl at temperature 300^0C to form trichlorosilane $SiHCl_3$ vapor. The chemical reaction follows equation (2.2).

$$Si + 3HCl \xrightarrow{300^0C} SiHCl_3 + H_2\uparrow \qquad (2.2)$$

Trichlorosilane TCS vapor is then gone to fractional distillation to remove unwanted impurities through a series of filters, condensers (boiling point 32^0C), and purifiers to finally get an ultra high purity liquid of purity higher than 99.9999999% at room temperature. The high-purity TCS is then used in the hydrogen reduction reaction at temperature $1{,}100^0$C to produce the electronic grade silicon EGS.

$$SiHCl_3 + H_2 \xrightarrow{1{,}100^0C} Si + 3HCl\uparrow \qquad (2.3)$$

The reaction takes place in a reactor containing resistance heated silicon rod, which serves as the nucleation point for deposition of EGS in polycrystalline form of high purity. This is the raw material used to prepare device quality single crystal. Pure EGS has impurity concentration generally in part per billion. The pure EGS is then ready to be pulled into silicon ingot for making wafer for integrated circuit fabrication.

There are a number of methods used to grow silicon crystalline ingot. We shall discuss two methods here namely Czochralski and Float-zone methods. Other methods such as horizontal zone furnace, which are Bridgeman-Stockbarger technique, liquid encapsulated Czochralski LEC are not discussed here.

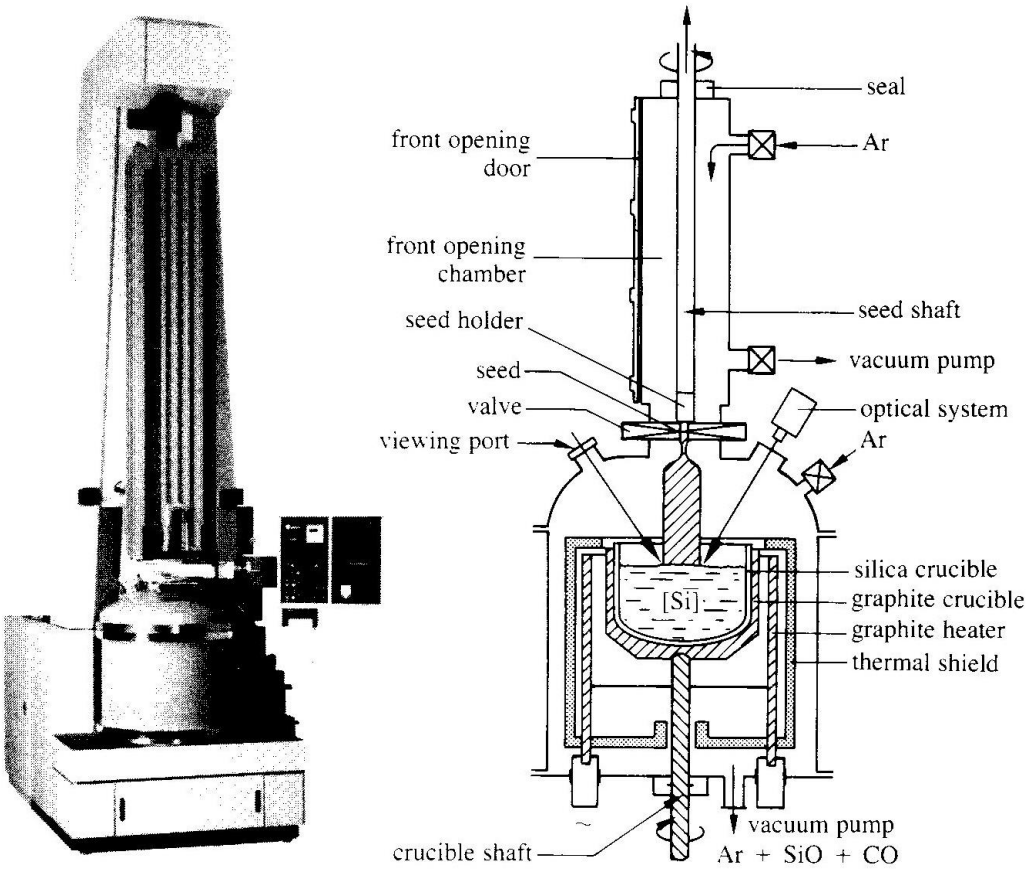
2.1.1 Czochralski Crystal Growth Method

The polycrystalline silicon is melt at temperature $1{,}415^0$C just above the melting point temperature of silicon, which is $1{,}414^0$C, in the argon Ar atmosphere in quartz crucible by radio frequency RF or resistive heating coil. Right type and the amount of dopant are then added. With the aid of “seed”, silicon rod of right diameter is formed by rotation and pulling in Czochralski CZ puller as shown in Fig. 2.1. Figure 2.1(a) shows the photograph of a modern computer-controlled Czochralski crystal puller. Figure 2.1(b) is the schematic drawing showing the components of the puller.

Once thermal equilibrium is established, the temperature at the vicinity of the seed is reduced and the molten silicon begins to freeze out onto the seed

crystal. Subsequently, the seed is slowly rotated and withdrawn at the rate of a few millimeter per minute to form a cylindrically shaped single crystal of silicon, which is known as *ingot*.

The diameter of the crystal in CZ method can be controlled by temperature and pulling rate using automatic diameter control system. Typically, 4 to 6 inch diameter and 1 to 2 meter in length type of ingot can be formed. In today's process, ingot of diameter as large as 12 inches is commonly produced to save cost and improve productivity. However, for large ingot as large as 12 inches in diameter, an external magnetic field is applied around the crucible and it is used to control the concentration of defects, impurities, and oxygen.



(a) Physical appearance (b) Internal structure

Figure 2.1: A Czochralski silicon rod puller

2.1.1.1 Impurity of Czochralski Process

The crystal ingot growth by Czochralski method always has trace impurities of oxygen and carbon, which come from silica and graphite crucible materials. Silica is silicon dioxide is the source of oxygen. Silica will react with graphite to form carbon monoxide, which is the source of carbon. The equation of chemical reaction is in equation (2.4).

$$SiO_2 + 3C \rightarrow SiC + 2CO \qquad (2.4)$$

Typically, the oxygen concentration is approximately ranged from $1.0x10^{16}cm^{-3}$ to $1.5x10^{18}cm^{-3}$ and the concentration of carbon varies from $2.0x10^{16}cm^{-3}$ to $1.0x10^{17}cm^{-3}$. The contents of oxygen and carbon are very much depending on ambient pressure, pulling and rotation rate, and the ratio of the diameter and the length of the ingot.

2.1.1.2 Concentration of Czochralski Process

In the crystal growth process, the most common dopants is boron and phosphorus, which are used to make *p*- and *n*-type semiconductor materials respectively. As the crystal is pulled from the molten silicon, the doping concentration incorporated into the crystal is usually different from the doping concentration of the molten silicon at the interface. The ratio of these two concentrations is defined as the *equilibrium segregation coefficient* k_0, which is defined in equation (2.5).

$$k_0 \equiv \frac{C_S}{C_I} \qquad (2.5)$$

where C_s and C_I are respectively the equilibrium concentration of the dopant in the solid and liquid near interface. Figure 2.2 shows the equilibrium segregation coefficient for common dopants used for silicon. The value below one means that during the growth the dopants are rejected into the molten silicon. As the result, the dopant concentration of molten silicon becomes higher as time lapsed.

Dopant	k_o	Type	Dopant	k_o	Type
B	$8.0x10^{-1}$	*p*	As	$3.0x10^{-1}$	*n*
Al	$3.0x10^{-3}$	*p*	Sb	$3.3x10^{-2}$	*n*
Ga	$8.0x10^{-3}$	*p*	Te	$3.0x10^{-4}$	*n*
In	$4.0x10^{-4}$	*p*	Li	$1.0x10^{-2}$	Deep-lying impurity level
O	1.25	*n*	Cu	$4.0x10^{-1}$	Deep-lying impurity level
C	$7.0x10^{-2}$	*n*	Au	$5.0x10^{-5}$	Deep-lying impurity level
P	0.35	*n*			

Figure 2.2: Equilibrium segregation coefficients for dopant in silicon

Consider a crystal being growth from the initial molten silicon of weight M_o with an initial doping concentration C_o (the weight of dopant per 1g of molten silicon) in the molten silicon. At a given time, a crystal of weight M has been grown, the amount of the dopant remaining in the molten silicon by weight is S. For an incremental amount of the crystal with weight dM, the corresponding reduction of the dopant -dS from the molten is $C_S dM$, where C_S is the doping concentration in the crystal by weight.

$$-dS = C_S dM \tag{2.6}$$

The remaining weight of the molten silicon is (M_o–M) and the doping concentration in liquid by weight C_I is given by

$$C_I = \frac{S}{M_o - M} \tag{2.7}$$

Substituting equation (3.6) and (2.7) into equation (2.5), it yields equation (2.8).

$$\frac{dS}{S} = -k_o\left(\frac{dM}{M_o - M}\right) \tag{2.8}$$

Given that the initial weight of the dopant C_oM_o, integration equation (2.8) yields equation (2.9).

$$\int_{C_oM_o}^{S} \frac{dS}{S} = -k_o\int_{0}^{M}\left(\frac{dM}{M_o - M}\right) \tag{2.9}$$

Solving equation (2.9) and combining equation (2.7), it yields equation (2.10).

$$C_S = k_o C_o\left(1 - \frac{M}{M_o}\right)^{k_0 - 1} \tag{2.10}$$

During the growth of silicon ingot, dopant is constantly being rejected into the molten silicon. If the rejection rate is higher than the rate at which the dopant can be transported away by diffusion or stirring, then a concentration gradient will develop at the interface as shown in Fig. 2.3. The equilibrium segregation coefficient is $k_0 = C_S/C_I(0)$. We can define an *effective segregation coefficient* k_e, which is the ratio of C_S and the impurity concentration far away from the interface.

$$k_e \equiv \frac{C_S}{C_I} \tag{2.11}$$

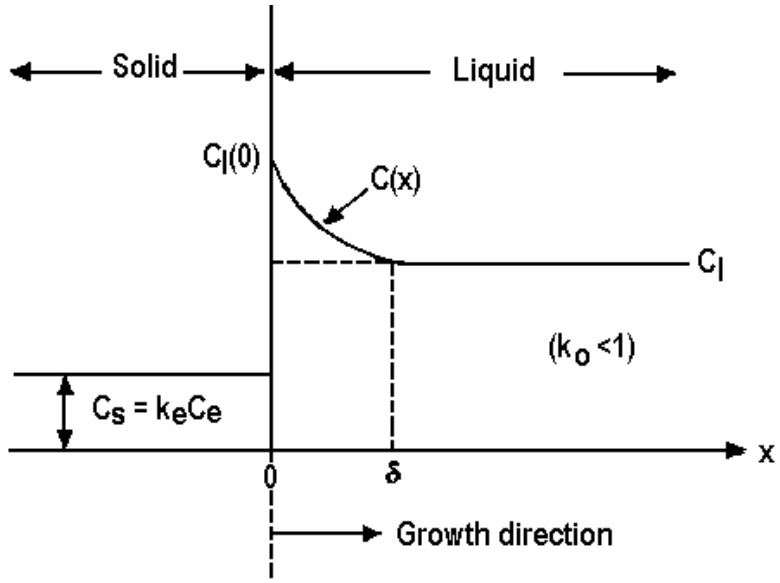


Figure 2.3: Doping distribution near the solid-molten interface

Consider a small virtual stagnant molten layer of width δ in which the only flow that required to replace the crystal being withdrawn from the molten. Outside the stagnant layer the concentration remains constant at C_I. In the layer, the concentration can be described by steady state continuation equation.

$$D\frac{d^2C}{dx^2} + v\frac{dC}{dx} = 0 \tag{2.12}$$

where D is the diffusion coefficient of the molten silicon and v is the velocity of the crystal growth. The solution of equation is C = $A_1 e^{-vx/D} + A_2$ with the constant to be determined by two boundary conditions. The first is at x = 0, C = $C_I(0)$ and second is determined by conservation of total number of dopant i.e. the sum of dopant flux at interface is zero. This condition yields equation.

$$D\left(\frac{dC}{dx}\right)_{x=0} + \left[C_I(0) + C_S\right] = 0 \tag{2.13}$$

Substituting the conditions and C = C_I at x = δ, the solution for the concentration C is

$$e^{-V\delta/D} = \frac{C_I - C_S}{C_I(0) - C_S} \tag{2.14}$$

The effective segregation coefficient k_e is

$$k_e = \frac{C_S}{C_I} = \frac{k_0}{k_0 + (1 - k_0)e^{-v\delta/D}} \tag{2.15}$$

2.1.1.3 Pull Rate of Czochralski Process

Pertaining pull rate of Czochralski crystal growth, one expects the pull rate should be slower for larger diameter ingot. Indeed the pull rate is inversely proportional to the square root of diameter of ingot. It can be derived based on the first order heat balance equation, which represents the dominant heat fluxes present during freezing process. Reference to Fig. 2.4, x_1 is a constant temperature surface, which is isotherm just inside the liquid. x_2 is an isotherm just inside the solid. During freezing process, which occurs between these isotherms, heat is released to allow the silicon to transform from liquid to solid state, which is heat of fusion. This heat must be removed from freezing interface. It is a primary process of heat transfer by conduction up to the solid ingot. Thus, one can write equation (2.16).

$$L\frac{dm}{dt} + k_L \frac{dT}{dx_1} A_1 = k_S \frac{dT}{dx_2} A_2 \tag{2.16}$$

where L is the latent heat of fusion, dm/dt is the amount of silicon freezing per unit time, k_L is the thermal conductivity of liquid, dT/dx_1 is the temperature gradient across the isotherm x_1, k_s is the thermal conductivity of the solid. dT/dx_2 is the temperature gradient across the isotherm x_2, and A_1 and A_2 are respectively the cross sectional areas.

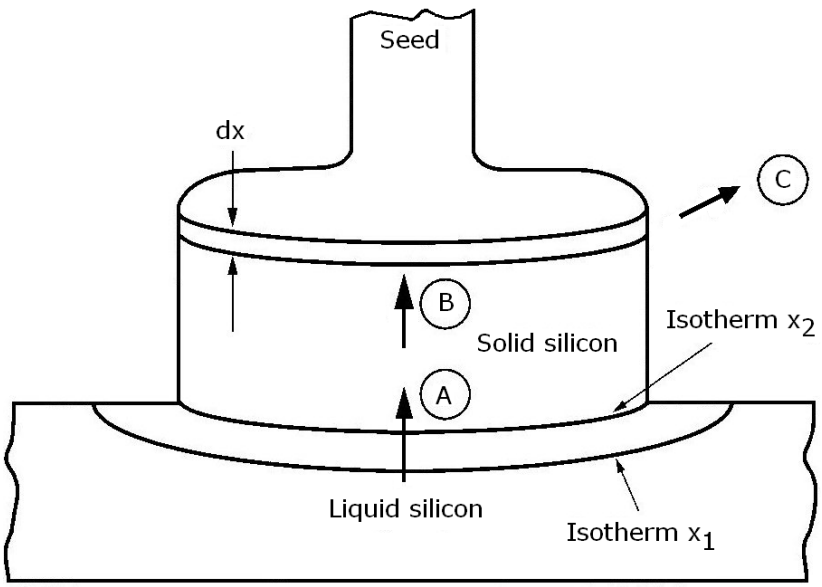


Figure 2.4: Freezing process occurring during Czochralski crystal growth

The middle term of equation (1.16) will drop from this point onward, which is representing any additional heat may flow from the liquid to the solid because of the temperature gradient between the two. By neglecting it, one can include only the absolute minimum heat which must be transported away from the freezing interface. The effect of this on the final result will be that the pull rate will be the maximum. If area A_1 and A_2 is equal to A then the rate of crystal V_p is pulled out of the molten silicon is simply equal to

$$\frac{dm}{dt} = V_p AN \tag{2.17}$$

Substituting equation (2.17) into equation (2.16) after ignoring the middle term of the equation, it becomes

$$V_{p_{MAX}} = \frac{k_s}{LN} \cdot \frac{dT}{dx_2} \tag{2.18}$$

V_{pMAX} is the maximum pull rate and N is the density of silicon.

In order to eliminate the temperature gradient term from equation (2.18), one needs to consider how the heat is conducted up the solid crystal and how it is eliminated from the solid ingot. Reference to Fig. 2.4, the latent heat of crystallization (A) is transferred from molten silicon to solid ingot. The heat is then transported away from the freezing interface primarily by conduction up the solid ingot (B). The heat is lost from ingot by radiation (C) and by convection, although one will consider only radiation to keep the analysis simple.

The Stefan-Boltzmann law describes heat loss due to radiation (C) is

$$dQ = (2\pi r dx)(\sigma\varepsilon T^4) \tag{2.19}$$

where $2\pi rdx$ represents the radiating surface area of an increment length of the ingot. σ is Stefan-Boltzmann constant and ε is the emissivity of the silicon.

The conducted up the ingot (B) is given by

$$Q = k_S\left(\pi r^2\right)\frac{dT}{dx} \tag{2.20}$$

where the πr^2 term is the cross sectional area of the ingot conducting the heat and dT/dx is the temperature gradient. Differentiating equation (2.20) yields

$$\frac{dQ}{dx} = k_S\left(\pi r^2\right)\frac{d^2T}{dx^2} + \left(\pi r^2\right)\frac{dT}{dx}\cdot\frac{dk_S}{dx} \cong k_S\left(\pi r^2\right)\frac{d^2T}{dx^2} \tag{2.21}$$

The second term in the derivative is normally neglected in comparison to the first term. Substituting equation (2.21) into equation (2.19), it yields equation (2.22).

$$\frac{d^2T}{dx^2} - \frac{2\sigma\varepsilon}{k_S}T^4 = 0 \tag{2.22}$$

This equation describes the temperature profile up to the solid ingot. The thermal conductivity of solid k_S varies approximately inverse of temperature i.e. 1/T at least for temperature below about $1{,}000^0$C. Thus, the conductivity of solid k_S is

$$k_S = k_M\frac{T_M}{T} \tag{2.23}$$

where k_M is the thermal conductivity at the melting temperature T_M. Thus equation (2.22) becomes equation (2.24) after substituting equation (2.23).

$$\frac{d^2T}{dx^2} - \frac{2\sigma\varepsilon}{k_M T_M}T^5 = 0 \tag{2.24}$$

This differential equation has solution, which is

$$T = \left(\frac{3k_M r T_M}{8\sigma\varepsilon}\right)^{\frac{1}{4}}\cdot\frac{1}{\sqrt{x + \left(\frac{3k_M r}{8\sigma\varepsilon T_M^3}\right)^{\frac{1}{2}}}} \tag{2.25}$$

Differentiating equation (1.25) with respect to x and evaluating the result for x = 0, which at freezing interface and substituting the result into equation (2.18), the maximum pull rate of the ingot is

$$V_{pMAX} = \frac{1}{LN}\sqrt{\frac{2\sigma\varepsilon k_M T_M^5}{3r}} \tag{2.26}$$

Equation (2.26) has clearly shown that the maximum pull rate V_{pMAX} is proportional to square root of the ingot's radius.

2.2.2 Float-Zone Crystal Growth Method

The float-zone crystal growth method is illustrated conceptually in Fig. 2.5. The crystal is not grown in the crucible that it has markedly reduced the impurity level particularly the level of oxygen and carbon. It is grown in sealed furnace with argon Ar gas. This method is used today for fabricating device that requires high resistivity and low oxygen content in the power device and detector device.

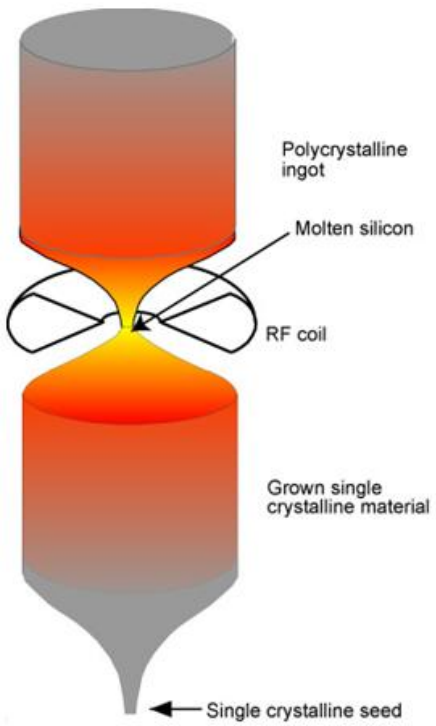


Figure 2.5: Basic float-zone crystal growth method

In the float-zone process, a polysilicon rod of EGS is clamped at both ends, with bottom in contact with a single-crystal seed. A small RF coil provides large current in silicon that locally melts the silicon. The molten zone is usually 2.0cm long. The liquid phase silicon is then bonded to the atomic plane of the seed plane by plane as the zone is slowly moved up. Doping of the crystal can be achieved by either starting with a doped polysilicon rod, a doped seed, or maintaining a gas ambient during the process that contains a dilute concentration of the desired dopant.

Segregation effect also plays an important role in the float-zone process just as it did in Czochralski method. It is illustrated from derivation of concentration of solid silicon $C_s(x)$ formed as it moves from molten state at the bottom to the top.

Figure 2.6 shows the idealized geometry of zone length L. The rod has initial concentration of C_0.

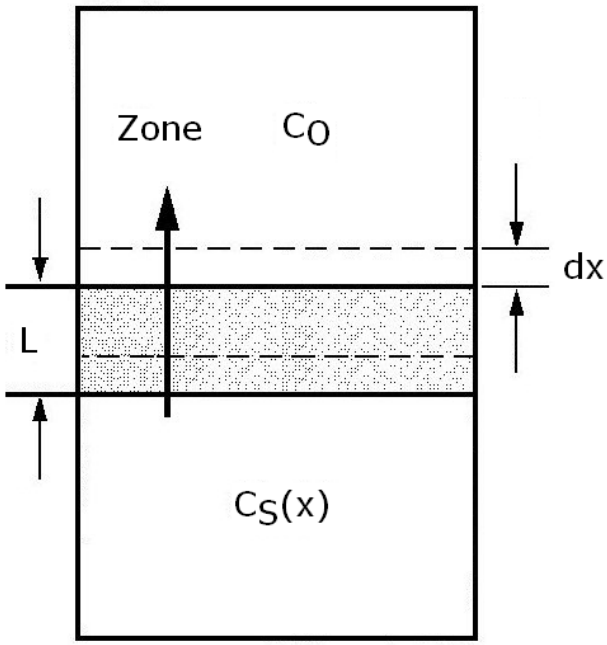


Figure 2.6: Float-zone crystal growth process from liquid zone at the bottom moving to top

If the molten zone moves upwards by a distance dx, the number of impurities in the liquid zone will change since some will dissolve into the melting liquid at the top and some will be lost to the freezing solid at the bottom. Thus,

$$dI = (C_0 - k_0 C_I)dx \tag{2.27}$$

where I is the number of impurities in the liquid. However, concentration of molten silicon is $C_I = I/L$. Thus, substituting it into equation (2.27) and integrating, it yields equation (2.28).

$$\int_0^x dx = \int_{I_0}^{I} \frac{dI}{C_0 - \frac{k_0 I}{L}} \tag{2.28}$$

where I_0 is the number of impurities in the zone when it is first formed at the bottom. Performing the integration and noting that $I_0 = C_0/L$ and $C_s = k_0 I/L$, the concentration of solid $C_s(x)$ at distance x is

$$C_S(x) = C_0\left[1-(1-k_0)e^{-\frac{k_0 x}{L}}\right] \tag{2.29}$$

As compared to Czochralski method, float-zone method has a greater resistivity variation. Thus, Czochralski method is still the dominant method for large diameter silicon crystal. The melt-crystal interface is very complex for float-zone method, so it is difficult to get dislocation free crystal. Unlike Czochralski method, it needs a high-purity polysilicon to begin.

2.2 Wafer Preparation

After the growth of silicon ingot, the ingot is machined cut at the end and polishes the sides to remove grooves created by automatic diameter control system. The flat of 150mm or smaller, or notch of 200mm or larger is grinded on the ingot to mark the crystal orientation.

The ingot is then sliced into wafer thickness of about 200mm using a rapid-rotating inward-diameter diamond-coated saw. After sawing, the wafer is grinded to round shaped edge to prevent edge chipping during mechanical handling of wafer processing.

The wafer is then rough polished by conventional abrasive, glycerin slurry with fine alumina Al_2O_3 suspension-lapping process to remove the majority of surface damage. It is necessary to create a flat surface for photolithography. The process can produce surface flatness within 2.0μm. During the lapping process, about 50μm of silicon is removed from both side of 200mm wafer.

After lapping process, a wet etch process is necessary to remove remaining damage that can be as deep as 10μm into the silicon. Thus, wet etch would remove 10μm from both sides of the wafer. The wet etchant is a mixture of nitric acid HNO_3, hydrofluoric acid HF, and acetic acid CH_3COOH. Nitric acid reacts with silicon to form silicon dioxide, while hydrofluoric acid then removes the oxide. Acetic acid is used to control the rate of reaction. The wet process further smoothen the surface due to isotropic etch characteristics with nitric acid-rich solution. The usual formation is a 4:1:3 mixture of nitric acid (79wt% in H_2O), HF (49wt% in H_2O), and pure acetic acid. The chemical reaction equation for the wet etch process is expressed in equation (2.30).

$$3Si + 4HNO_3 + 6HF \rightarrow 3H_2SiF_6 + 8H_2O + 4NO\uparrow \tag{2.30}$$

The last process is mechanical-chemical polishing CMP as shown in Fig. 1.12. The wafer is held on a rotating holder and pressed on a rotating polishing pad with slurry and water in between. The slurry is a colloidal suspension of fine silica SiO_2 particle with diameter of about 100 Å in an aqueous solution of sodium hydroxide. Sodium hydroxide oxidizes, which is a chemical process, the silicon surface with the help of heat generated by friction between wafer and polishing pad. The silica particle then abrades the silicon dioxide away from the surface – a mechanical process.

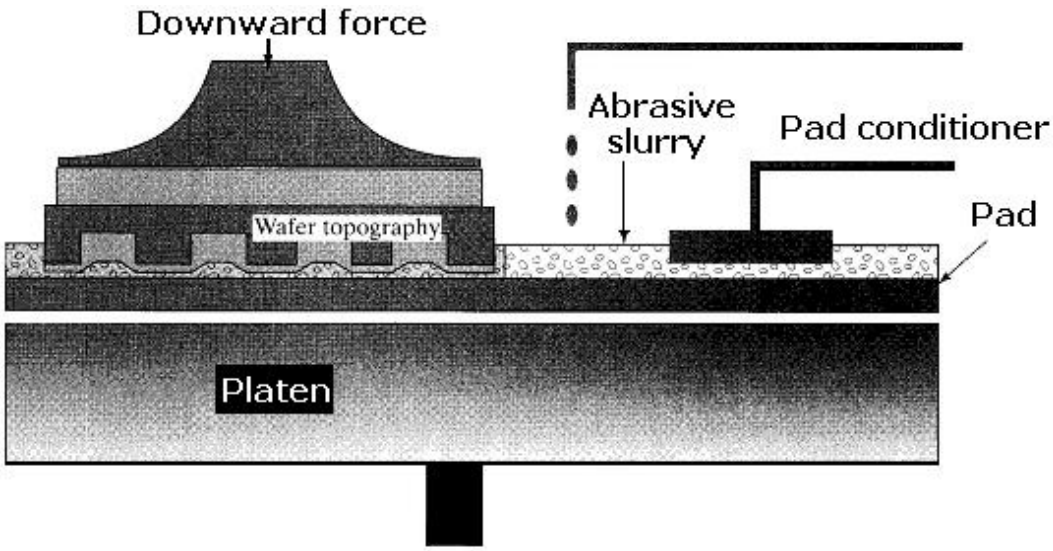


Figure 2.7: Chemical mechanical polishing technique

The post CPM process is a cleaning process with a mixture of acid-oxidizer solution to remove organic and inorganic contaminant and particles (RCA clean 1 and clean 2 solutions). The finished wafer has a defect-free surface ready for IC fabrication.

At the back of wafer, defect and dislocation are intentionally created to trap heavy metal, mobile, oxygen, carbon, and other alkaline contaminant as mentioned in earlier Section. Back side defect can also be created using argon ion implantation, polysilicon deposition, and heavily doped phosphorus. During fabrication, the backside of the wafer is usually always deposited with a chemical vapor deposition CVD silicon dioxide or silicon nitride Si_3N_4 layer to prevent any out diffusion during thermal process.

Exercises

2.1. The seed crystal used in Czochralski process is usually necked down to a small diameter of 5.5mm as a means to initiate dislocation-free growth. If

the critical yield strength of silicon is $2.0 \times 10^6 g/cm^2$, calculate the maximum length of a silicon ingot 200mm in diameter that can be supported by such a seed. Given the density of the silicon ingot is $2.33 g/cm^3$.

2.2. A silicon ingot contains 2.0×10^{18} phosphorus atoms cm^{-3} is to be grown by the Czochraski technique. Given that the density of molten silicon is $2.53 gcm^{-3}$, the atomic weight of phosphorus is 30.97g, and the segregation coefficient of phosphorus is 0.35.

(i). What is the concentration of phosphorus atoms should be in the molten silicon to give the required concentration in ingot?

(ii). If the initial load of silicon in crucible is 150.0kg, how many grams of phosphorus should be added?

2.3. A silicon ingot contains 10^{16} boron atoms cm^{-3} is to be grown by the Czochraski technique. The initial load of silicon in crucible is 60kg. After 60% of the molten silicon has been converted into solid silicon, what is the amount of solid silicon required to be added to the molten silicon so that it can get back its initial concentration?
Given the following
Density of molten silicon is $2.53 gcm^{-3}$.
Density of solid silicon $2.32 gcm^{-3}$.
Atomic weight of silicon is 28.08g.

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