Fabrication and Characterization of Nanomaterials

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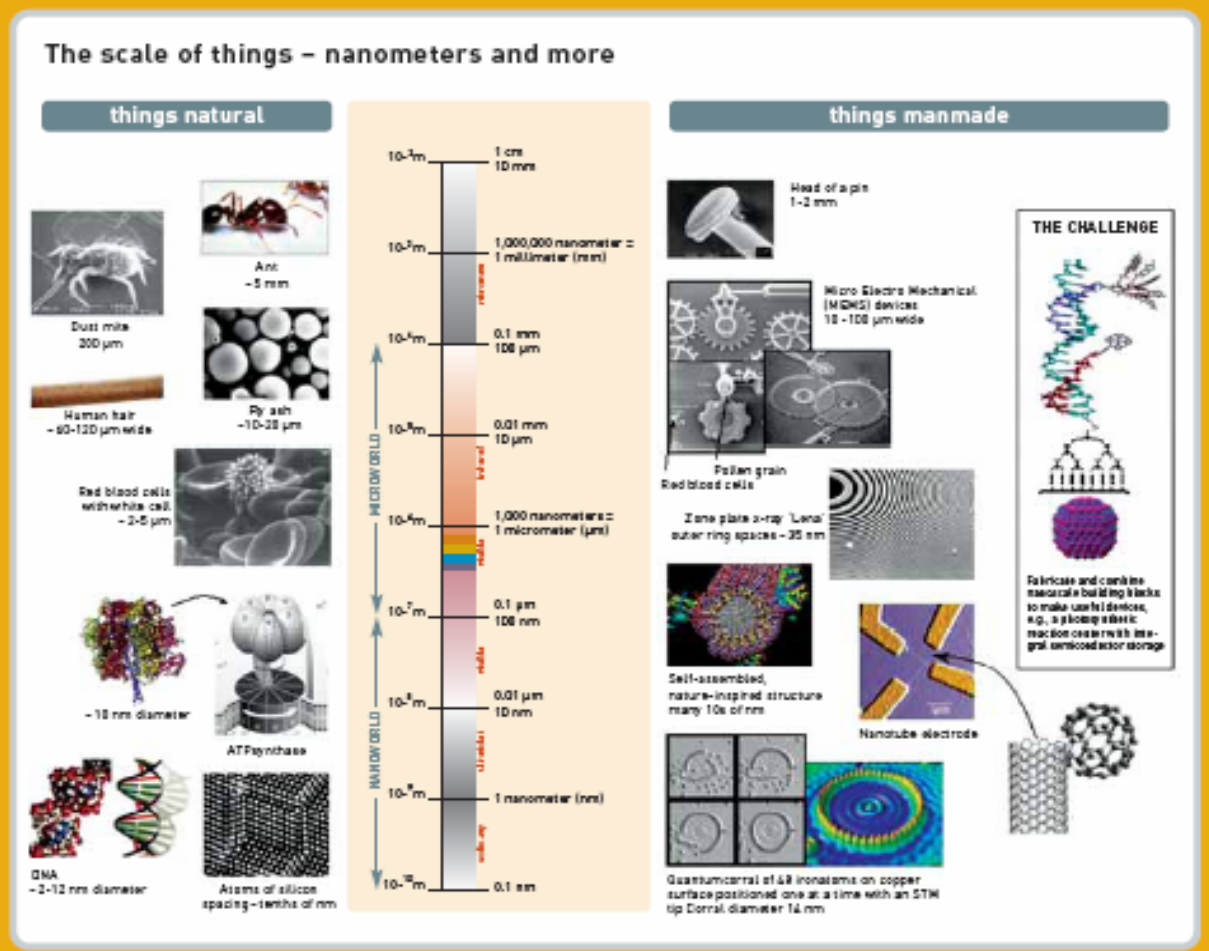
Fabrication and Characterization of Nanomaterials Outline of Opening Lecture

- Why physics changes at the nanoscale
- Examples of nanoscale devices, circuits, and systems
- General semiconductor IC fabrication methods and limitations
- Need for metrologies to support semiconductor fabrication, performance evaluation, failure analysis, and reliability assessment
- Types of metrologies
- Wrapup and future challenges


The scale of things – nanometers and more
things natural
things manmade
Dust mite
200 µm
Ant
~5 mm
Human hair
~60-120 µm wide
Fly ash
~10-30 µm
Red blood cells
with white cell
~2-5 µm
~10 nm diameter
ATPsynthase
DNA
~2-12 nm diameter
Atoms of silicon
spacing ~tenths of nm
10⁻¹m
1 cm
10 mm
10⁻²m
1,000,000 nanometer =
1 millimeter (mm)
10⁻³m
0.1 mm
100 µm
10⁻⁴m
0.01 mm
10 µm
10⁻⁵m
1,000 nanometers =
1 micrometer (µm)
10⁻⁷m
0.1 µm
100 nm
10⁻⁸m
0.01 µm
10 nm
10⁻⁹m
1 nanometer (nm)
10⁻¹⁰m
0.1 nm
MICROWORLD
NANOWORLD
Head of a pin
1-2 mm
Micro Electro Mechanical
(MEMS) devices
10 - 100 µm wide
Pollen grain
Red blood cells
Zone plate x-ray "Lens"
outer ring spacing ~35 nm
Self-assembled,
nature-inspired structure
many 10s of nm
Nanotube electrode
Quantum corral of 48 iron atoms on copper
surface positioned one at a time with an STM
tip Corral diameter 14 nm
THE CHALLENGE
Fabricate and combine
nanoscale building blocks
to make useful devices,
e.g., a photosynthetic
reaction center with inte-
gral semiconductor storage

- 6 -

Why physics changes at the nanoscale

- Surface area/volume ratio increases as 1/R and the surfaces and interfaces become the major contributor to materials properties, thermodynamic behavior, and energy carrier dynamics at the nanoscale
- Diffusion of atoms to surfaces and interfaces changes the thermodynamic equilibrium conditions
- Solid transport of heat, matter, charge carriers, photons, -- all change at the nanoscale because the scattering centers are spaced further apart than the nanoscale dimensions
- Electronic density of states becomes discontinuous when dimensions are reduced to quantum wells, quantum wires, and quantum dots. This leads to new physical concepts such as energy filtering, carrier “pocket engineering”, and electronic transitions (such as semimetal-semiconductor transitions)
- Size-dependent energy levels due to quantum confinement change the energetics of doping semiconductor nanocrystals
- Fluid transport in nanoscale channels can be enhanced by atomic smoothness, contact angle changes, and molecular ordering of the molecules being transported

Why physics changes at the nanoscale

- Terascale semiconductor device densities lead to new nanoscale problems:
  - Overlap of electric fields causes threshold voltage lowering in devices and parasitic signal transfer in interconnects
  - Tunneling induced leakage causes excessive charge loss across very thin dielectrics (increases exponentially as 1/thickness)
  - Excessive heat generation due to the inherent switching energy governed by thermodynamics (~100kTln2 = 1.7eV/switch at R.T. so that for 0.1ps switching time at $10^{12}/cm^2$ density there will be $3x10^4$ W/cm^2 dissipated vs. $3x10^2$ W/cm^2 max dissipated by convection cooling)
  - Charge transport becomes affected by lattice phonon scattering
  - Doping becomes problematic due to quantum confinement effects and to outdiffusion to surfaces and interfaces (self-purification)

Why physics changes at the nanoscale

- Carriers of heat, charge, and matter at the macroscale are governed by statistical distribution of scattering
- These govern phenomena such as thermal management, electrical charge transport, and diffusion of dopants
- These carriers include phonons, electrons, photons, and atoms
- This leads to governing equations for the distribution of carriers such as:
  - Fermi-Dirac for electron probability density
  - Bose Einstein for photon and phonon probability density
  - Maxwell distribution for electromagnetic radiation
  - Boltzmann distribution for temperature dependence of atoms and molecules energies

Why physics changes at the nanoscale

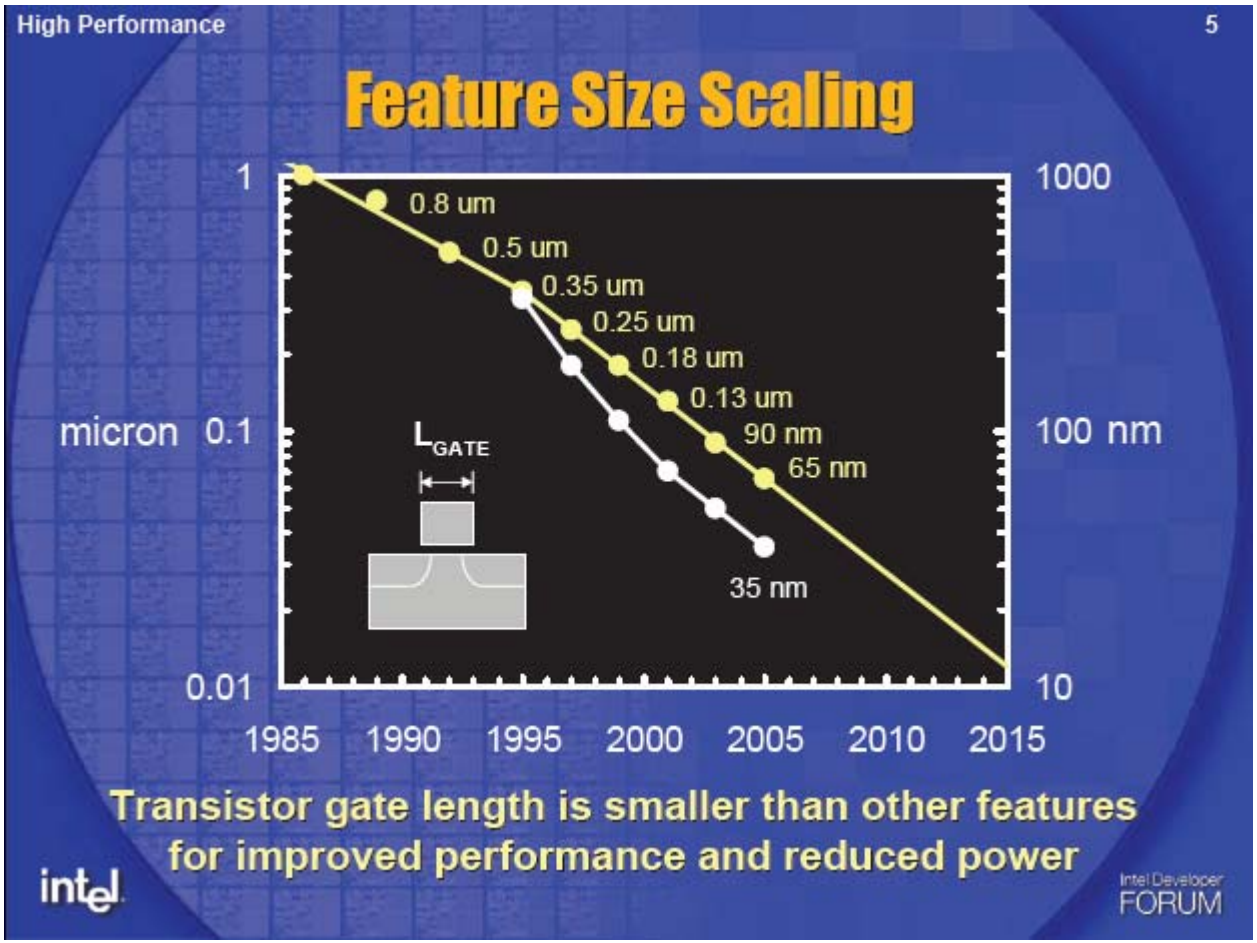
- As we approach dimensions where the carrier mean free paths are longer than the size of the nanoscale object, everything changes
- We must consider whether to treat the carriers as particles or waves according to the principles of quantum mechanics
- Typical mean free paths are:
  - Electrons and phonons – 10 - 100nm
  - Photons – wavelengths from 0.01nm to 1km
  - Atoms – interatomic distances – 0.1nm to 0.5nm
- When mean free paths are greater than nanoscale object dimensions, we use wave equations, when less we use particle equations
- Thus at the nanoscale the following governing transport equations apply:
  - Photons – radiative transfer => Maxwell equations
  - Electrons – Ohm's Law => Boltzmann transport => ballistic transport
  - Phonons – Fourier's Law => Boltzmann transport => ballistic transport
  - Atoms – Fick's Law => Boltmann transport => ballistic transport

Why physics changes at the nanoscale

- Implications for the design and fabrication of nanoscale devices
  - Charge carriers in FET's – ballistic transport in the channels, tunneling across the gate dielectrics (such effects lead to reliability problems)
  - Phonon coupling to electrical carriers and surface proximity are new scattering sources
  - Overlapping electric fields – drain induced barrier lowering, impedance in interconnects
  - Thermal conduction is reduced by interface scattering and decoupling of phonon-electron interactions
  - Power dissipation – switching energy is fixed at 1E-19 J/switch by physics so that for gigascale and terascale density levels, the heat generated can be very high if all transistors switch simultaneously
  - Fabrication is dominated by process variability due to narrow limits of statistical process control
  - Defects levels increase exponentially at smaller defect sizes such as particles and process variability – from ppm to percent levels
  - Device issues from physics and fabrication require new architectural approaches to perform useful computing functions

Examples of Nanoscale Devices, Circuits, and Systems

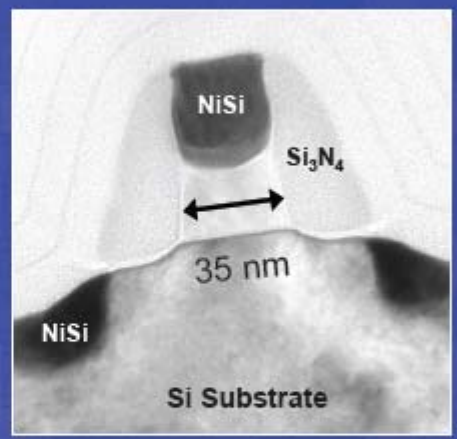
- Microprocessors => nanoprocessors with multicores and multithreads, with redundancy and reconfigurability
- Functional CMOS with embedded non-volatile, ultra-high density nanoscale memory
- Nanoscale sensors based on detection of biomolecule binding events by electrical charge and spin, and photonics (evanescent waves and plasmonics)
  - Protein antibody-antigen binding
  - Receptor-ligand binding
- Typical nanosensors include quantum dots, optical resonators, semiconductor nanowires, carbon nanotubes, nanoporous membranes, --


High Performance
5
Feature Size Scaling
1
micron
0.1
0.01
1000
100 nm
10
0.8 um
0.5 um
0.35 um
0.25 um
0.18 um
0.13 um
90 nm
65 nm
35 nm
L_{GATE}
1985
1990
1995
2000
2005
2010
2015
Transistor gate length is smaller than other features
for improved performance and reduced power
intel
Intel Developer
FORUM

High Performance 6

65 nm Generation Transistors

- 35 nm gate length
- 1.2 nm gate oxide
- NiSi for low resistance
- 2ND generation strained silicon for enhanced performance



Leading edge transistor technology is unmatched by our competitors

intel

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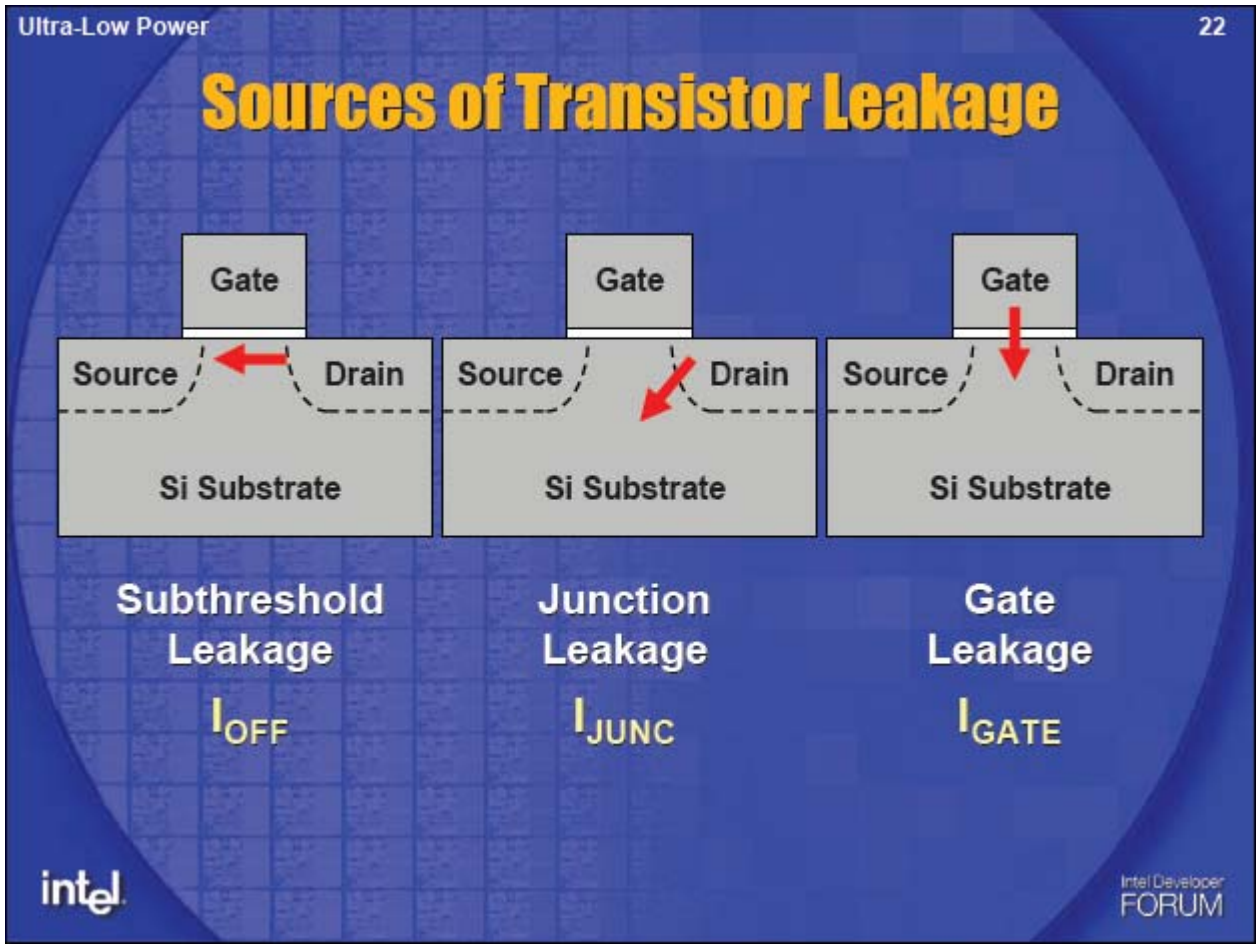
Ultra-Low Power
22
Sources of Transistor Leakage
Gate
Source
Drain
Si Substrate
Gate
Source
Drain
Si Substrate
Gate
Source
Drain
Si Substrate
Subthreshold Leakage
I_{OFF}
Junction Leakage
I_{JUNC}
Gate Leakage
I_{GATE}
intel
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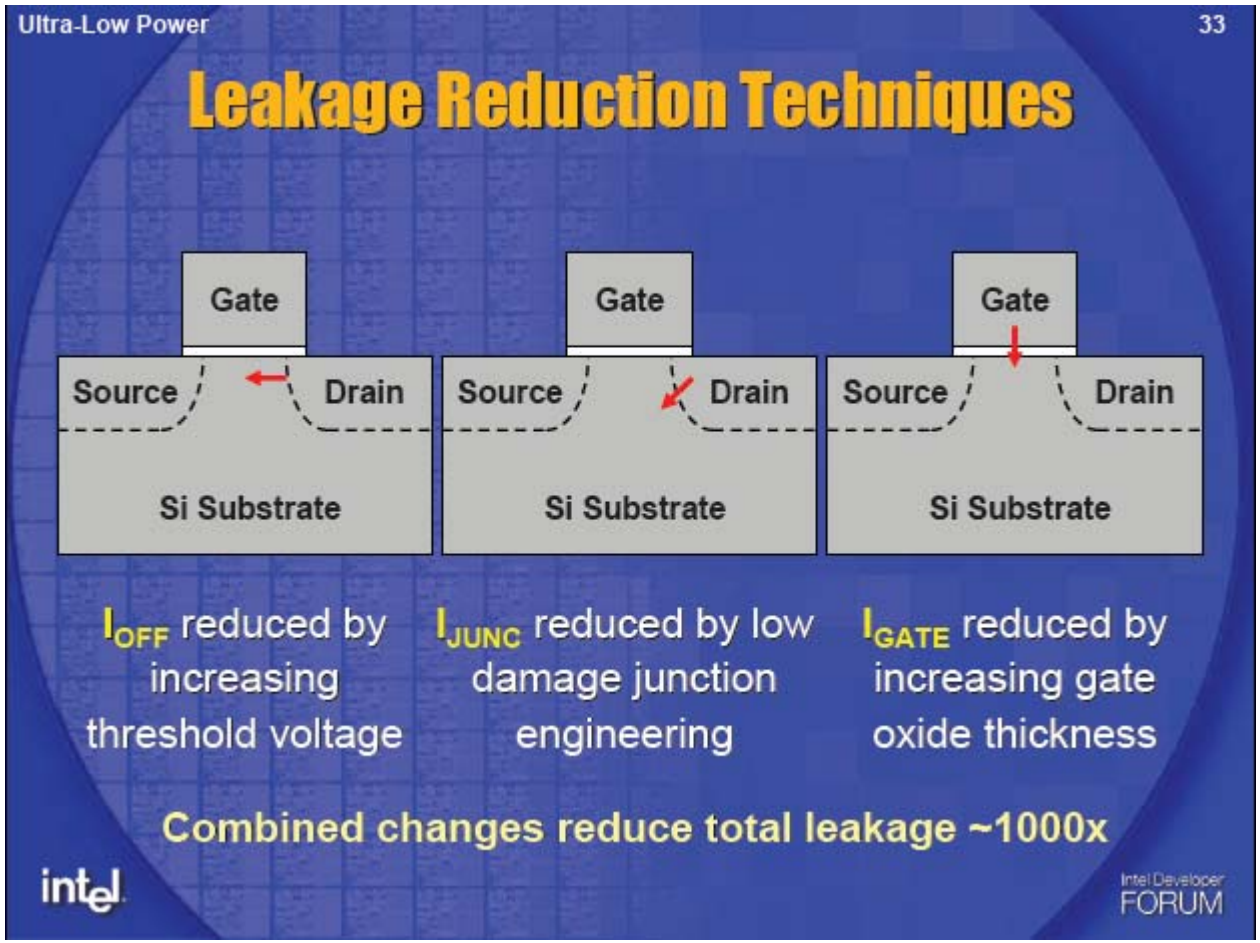
Ultra-Low Power
33
Leakage Reduction Techniques
Gate
Source
Drain
Si Substrate
Gate
Source
Drain
Si Substrate
Gate
Source
Drain
Si Substrate
I_{OFF} reduced by increasing threshold voltage
I_{JUNC} reduced by low damage junction engineering
I_{GATE} reduced by increasing gate oxide thickness
Combined changes reduce total leakage ~1000x
intel
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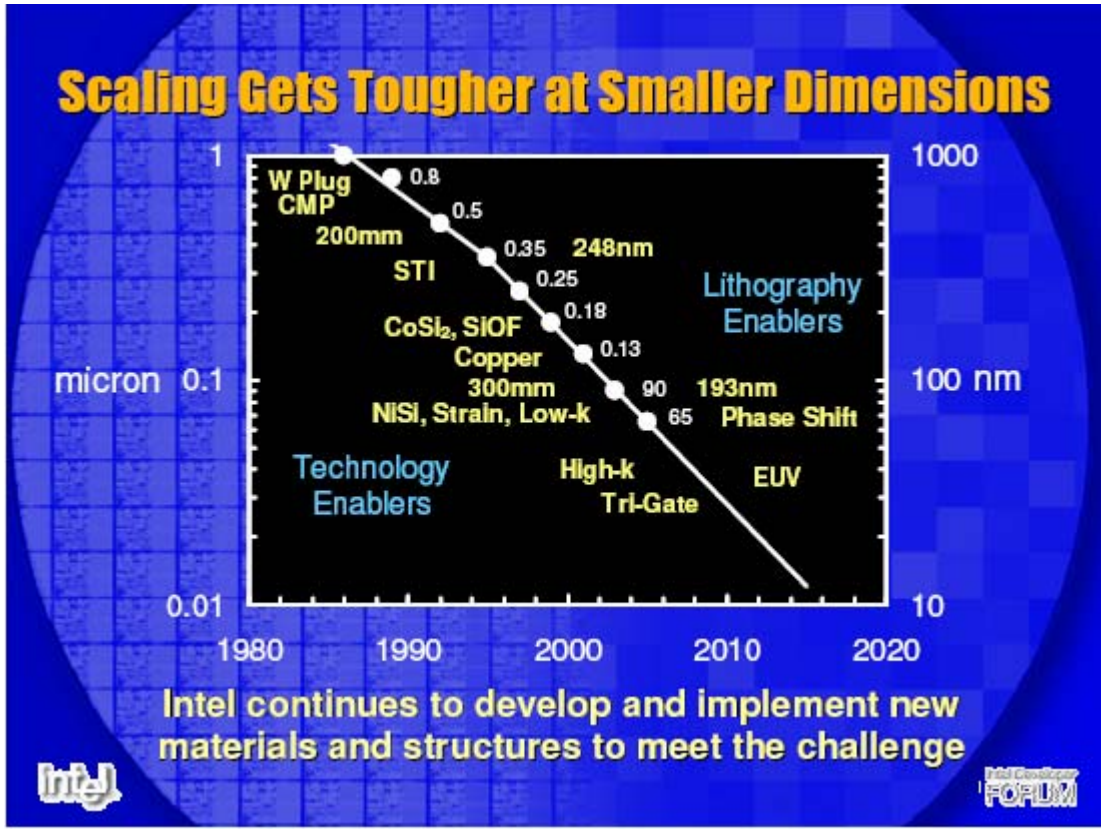
Scaling Gets Tougher at Smaller Dimensions
1
micron
0.1
0.01
1000
100 nm
10
1980
1990
2000
2010
2020
W Plug CMP
200mm
STI
CoSi2, SiOF
Copper
300mm
NiSi, Strain, Low-k
0.8
0.5
0.35
0.25
0.18
0.13
90
65
248nm
193nm
Phase Shift
Lithography Enablers
Technology Enablers
High-k
Tri-Gate
EUV
Intel continues to develop and implement new materials and structures to meet the challenge
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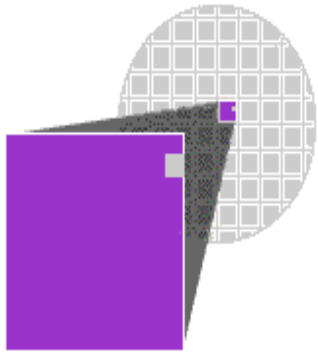
FORUM

General Semiconductor IC Fabrication Methods and Limitations

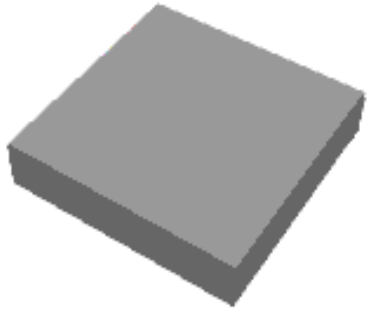
- Front end processing
  - Fabrication of transistors and local interconnects on 300mm silicon wafers
- Back end processing
  - Fabrication of on-chip interconnect lying on top of the transistor layers
- Test
  - Check for major defect issues
- Packaging
  - Wafer cut into die, die attached to package substrate, package level interconnect added to interface with external connections
- Final Burn-in and Test
  - Check for system faults after burn-in to remove early fails

General Semiconductor IC Processing Methods and Limitations

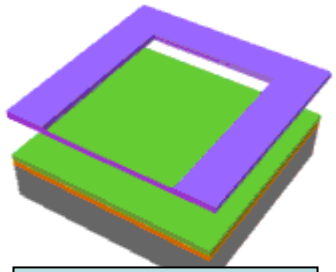
- Processes developed over the last 50 years are “top-down”, meaning that they modify the surfaces in some important ways to build up transistor and interconnect structures
- Typically there are five methods applied sequentially in a monolithic manner through a series of >250 individual steps:
  - Oxides or epitaxial films are grown on the silicon substrates (300mm diameter)
  - Materials are deposited in the form of thin films, implanted ions, diffusion sources
  - The surfaces are planarized so that the height differences will be smaller than the depth of focus of the optical lithography tool
  - The surfaces are patterned using some form of photolithography with resists and masks
  - The surfaces are etched using plasma chemistries or wet etches to remove unwanted material



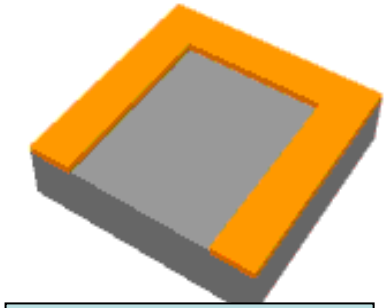
Wafer layout



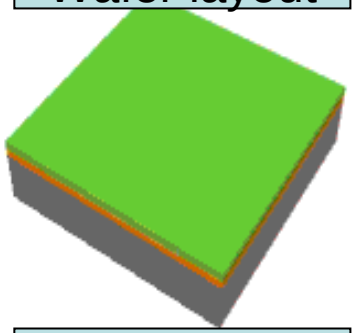
SiO2 Growth



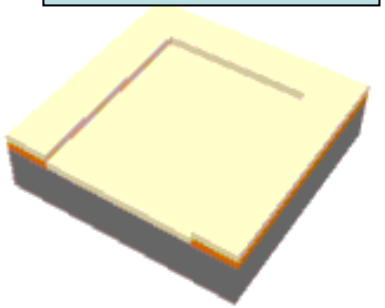
First mask



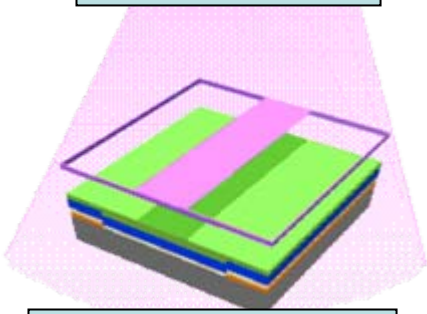
Dissolve SiO2



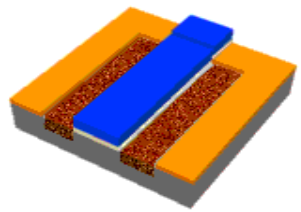
Resist spin



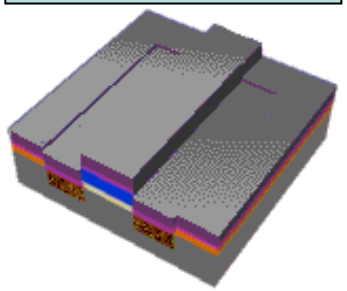
Polysilicon Layer



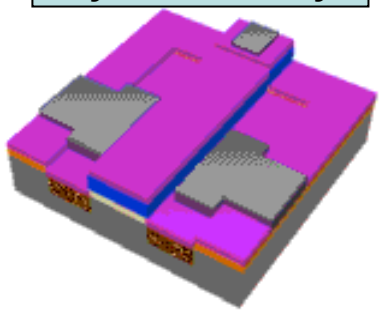
Second mask



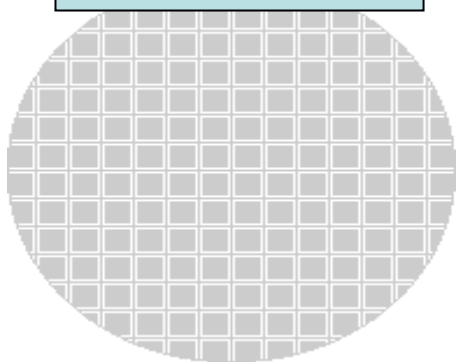
Implant



First metal



Second metal
(of 20 layers)



Wafer dice for assembly

Package/test

General Semiconductor IC Fabrication Methods and Limitations

Limitations

- Lithography
  - Feature sizes are less than the wavelength of the light used
  - Masks require complex proximity correction and phase control features
  - Resists suffer from internal diffusion of the photoactive components
  - Line edge roughness approaches feature sizes below 35nm
  - High numerical aperture of optics deceases the useable depth of focus
  - Cost and complexity increase
- Gate oxide growth
  - SiO_2 gates suffer from leakage due to tunneling and must be replaced by higher dielectric constant oxides that are not natural to silicon
- Thin film deposition
  - Chemical vapor deposition must be replaced by atomic layer deposition to obtain the needed coverage and low defect density
- Etching high aspect ratios
  - Etch selectivity needs to be increased to allow high aspect ratio features
- Ion implantation of dopants
  - Ion damage become serious
  - Dopant flux is too high to allow low doping level control
- Planarizing surfaces
  - Different surface materials polish at different rates thus causing surface relief features that are larger than the depth of focus

General Semiconductor IC Fabrication Methods and Limitations

Overall Limitations with Current Processing

- Process variability
- Materials stability
- Interface control
- Mask layer alignment and registration from layer to layer

General Semiconductor IC Fabrication Methods and Limitations

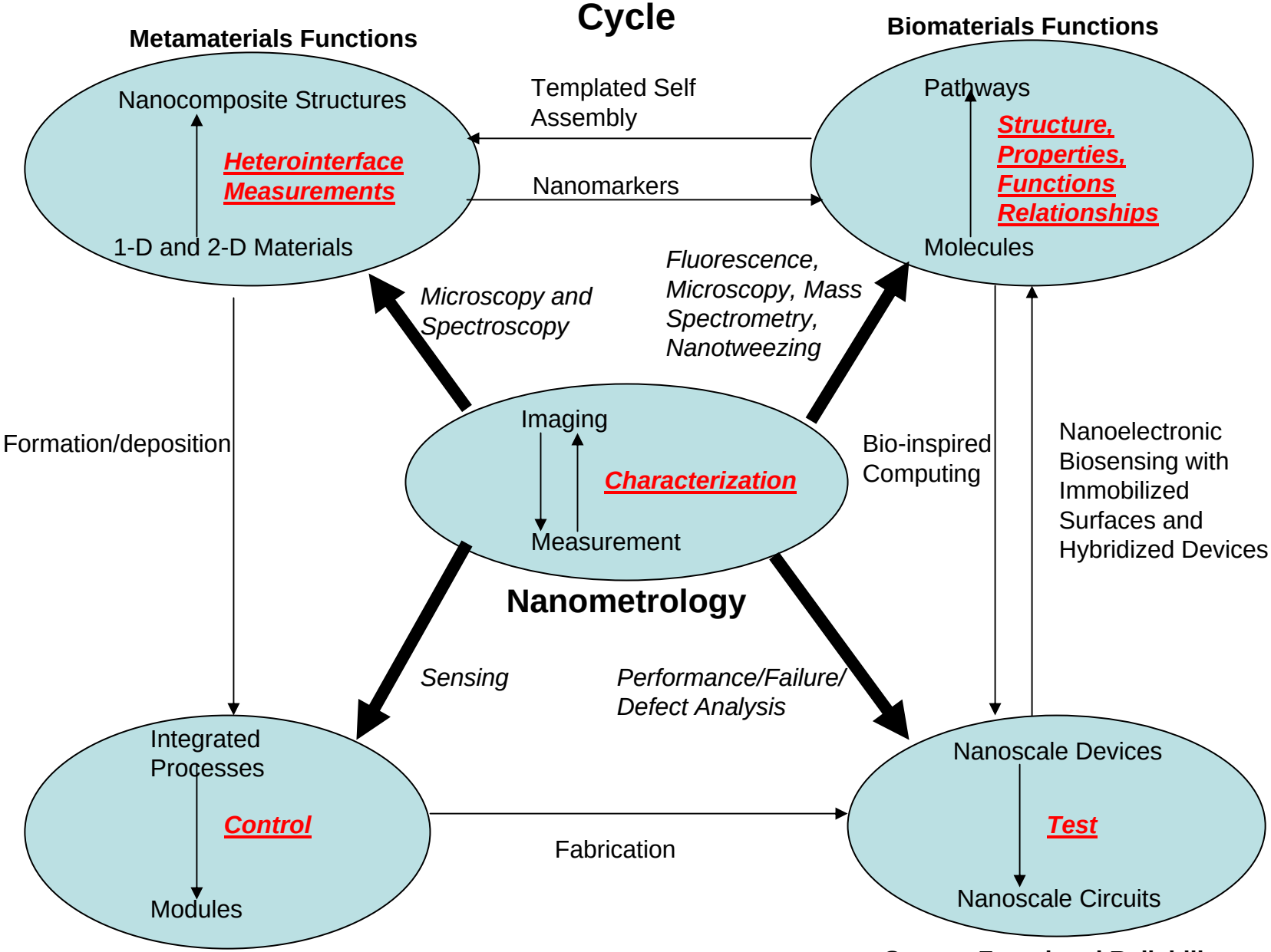
Bottoms-up Fabrication

- Idea is to build templates on the surface of the wafer that serve as “masks” for subsequent processing
- Technique called directed self-assembly
- Templates include porous oxides, DNA constructed particles, block copolymers, ion implanted damage, --
- Layout of features is can be either aperiodic or regular but cannot be formed into the multitude of shapes and sizes required for the layout of logic devices and circuits
- So far this method has been proposed for very high density memory elements that can be randomly distributed and connected by interconnect multiplexing methods
- Not yet demonstrated for any manufacturing

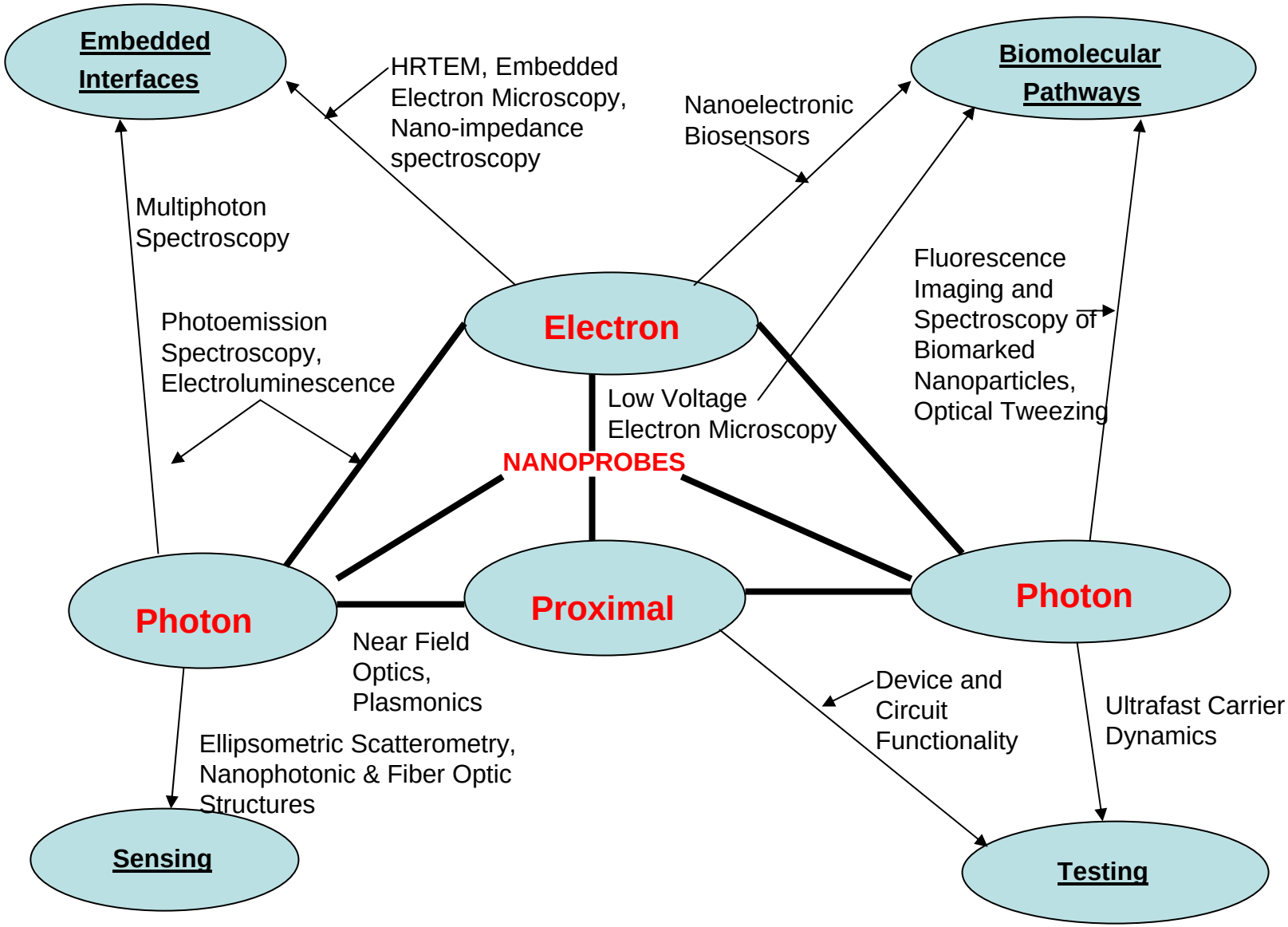
Nanometrologies

- Metrologies are needed in order to image and measure the properties of nanoscale objects
- Without capabilities such as electron microscopes, we would not have the microscale technologies we have today
- Similarly, we need measurement capabilities at the nanoscale, otherwise we will not be able to manufacture terascale circuits or validate their operational performance and reliability
- Capabilities can be separated by the probes used:
  - Charged particle probes (TEM, SEM, Ion probes)
  - Proximal probes (STM, AFM, SPM)
  - Electromagnetic probes (NSOM, Confocal microscopy)

ONAMI Integrated Nanometrology Interdependency Cycle



Integrated Nanometrology Capabilities and Applications



What and How do we Measure at the Nanoscale?

- Nanoscale materials, device, and Interface properties
  - Photon based materials – nano-optic structures, plasmonic materials
  - Charge- and spin-based – nanoionics, organic semiconductors
  - Fabrication and interfaces – heterostructure nanowire thermal transport, nanolaminated structures, ink-jet printing of nanoscale films, metal contacts to carbon nanotubes
- New nanoscale metrology techniques
  - Structure and composition – SIMS nanotomography, nanostructuture identification, THz spectroscopy of biomolecules, optical tweezing and single molecule spectroscopy
  - Transport carriers – electron wave probes, near field optical imaging od charge carriers and plasmons
  - Surfaces and interfaces – microwave STM, shear force AFM, ellipsometer/AFM imaging, photoemisison at high resolution

Oregon Nanoscience and Microtechnologies Institute (ONAMI)

What is ONAMI?

- Research collabration in the micro and nanosciences and engineering among the 3 Oregon research universities (PSU, UO, OSU)
- Funded by the State of Oregon with support from the Oregon Congressional Delegation
- Three major thrusts/leaders:
  - Tactical energy systems based on microscale technologies – Prof. Kevin Drost, OSU
  - Green nanomanufacturing – Prof. Jim Hutchison, UO
  - Nanometrology and nanoelectronics – Prof. John Carruthers, PSU

ONAMI Nanometrology and Nanoelectronics FY06 Initiative

- Nanometrology
  - Charged Particle Probes
    - Quantum Electron Wave Probes, SIMS Nanotomography, Lattice Fringe Structure Fingerprinting
  - Proximal Probes
    - RF STM, Shear Force AFM
  - Photon (electromagnetic) Probes
    - THz Spectroscopy, Simultaneous Optical and Tomographic Nanoscale Imaging, High Resolution Photoemission Microscopy, Optical Properties of Nanoscale Materials, Nanoionics, Near Field Optical Imaging of Carriers and Plasmons
- Nanoelectronics
  - Charge Based Devices
    - Charge Carrier Dynamics in Nanoscale Organic Semiconductors, Thermal Conductance of Heterostructure Nanowires
  - Spin Based Devices
    - Reconfigurable Magnetoresistive Devices with ALD MgO Tunneling Layers
  - Photon Based Devices
    - Active Plasmonic Materials, Optical Field Enhancement in Tweezer Trapping and Single Molecule Spectroscopy
- Applications
    - Ferromagnetic Resonance Biosensors, Nanolaminated Structures
- Nanofabrication
    - Inorganic Ink Jet Printing, Carbon Nanotube Based Devices

ONAMI at PSU

- Center for Electron Microscopy and Nanofabrication in SB1 – Director, Prof. Jun Jiao, Dr. Chunfei Li
- Physics
  - SPM and NSOM – Prof. Andres LaRosa and Prof. Erik Sanchez
  - Optical spectroscopy – Prof. John Freeouf
  - Nanoscale materials structure determination – Prof. Peter Moeck and Prof. Bjorn Siepel
  - Photoemission spectroscopy and microscopy – Prof Koenenkamp and Prof. Gert Rempfer
  - Nanoscale semiconductor materials, processes, and devices – Prof. Raj Solanki, Prof. Jun Jiao, Prof. Rolf Koenenkamp

ONAMI at PSU

- Chemistry
  - Surface chemistry and immobilization – Prof. Mingdi Yan
  - Resist and organic chemistry – Prof Shankar Rananavare
  - Bio Sensors – Prof Scott Reed
- Electrical Engineering
  - Nanoscale computer architectures – Prof. Dan Hammerstrom
  - Device modeling – Prof. Brano Pejcinovic and Prof. Malgorzata Jeske
  - Quantum dot structures – Prof Jim Morris
  - Circuit testing – Prof. Rob Daasch
  - Nanoscale biosensors – Prof. Shalini Prasad
- Mechanical Engineering
  - Thermal transport at the micro/nanoscale, nanotribology – Prof. Mark Weislogel
  - Modeling of transport phenomena – Prof. Lemmy Meekisho

Opportunities in Nanotechnology

- In general the fields are
  - Nanomaterials – nanocomposites, nanoparticles
  - Nanodevices – semiconductors, storage, sensing
  - Nanomeasurements – microscopy and spectroscopy instruments
- Remember that nanomaterials and devices must integrate into the real world – this requires engineering based on solid physics, chemistry and biology
  - Portable systems – computing, communications, sensing, power
  - Design tools are needed across all these heterointegration boundaries – based on real physical principles
  - Packaging and testing models will be needed
  - Reliability of these multifunctional microsystems is an emerging issue
- But the keys to job opportunities are networking with other people and companies, universities, or national labs and continued learning
  - Attend technical society meetings and network with others
  - Be aggressive in learning more – through googling and literature searches
  - Be knowledgeable about companies/labs where you are interviewing
  - Show how your ideas and knowledge can benefit those companies/labs
  - Be prepared by continuous learning for multiple career changes as the technology matures and changes